REMARKS/ARGUMENTS

Amendments were made to the specification to update the status of related applications identified on pages 1 and 2 thereof. No new matter has been added by any of the amendments to the specification.

Claims 1, 3-18, 20-23 and 25 are pending in the present application. Claims 1, 3, 5, 11, 18, 20, 23 and 25 were amended; and claims 2, 19 and 24 were canceled. No claims were added. Applicants have carefully considered the cited art and the Examiner's comments and believe the claims patentably distinguish over the cited art and are allowable in their present form. Reconsideration of the rejection is, accordingly, respectfully requested in view of the above amendments and the following comments.

I. Double Patenting

The Examiner has provisionally rejected claim 1 on the grounds of nonstatutory double patenting over claim 1 of copending Application Nos. 10/675,778; 10/675,776; and 10/675,721, and over claim 2 of copending Application No. 10/675,872.

By the present Amendment, claim 1 has been amended to incorporate subject matter recited in claim 2, and claim 2 has been canceled. Accordingly, the provisional rejection of claim 1 on the grounds of nonstatutory double patenting has been overcome.

II. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1-3, 15, 17, 18-20 and 22-25 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,754,839, to Pardo et al. (hereinafter "Pardo"). This rejection is respectfully traversed.

Claim 1 as amended herein is as follows:

> 1. A method in a data processing system for processing instructions, the method comprising:
>
> responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction;
>
> enabling counting of each event associated with execution of the instruction if the indicator is associated with the instruction; and
>
> counting each event associated with the execution of the instruction if counting is enabled for the instruction.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single prior art reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of a claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product

or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983).

Applicants respectfully submit that Pardo does not identically show every element of the claimed invention arranged as they are in the claims; and, accordingly, does not anticipate the claims. With respect to claim 1, in particular, Pardo fails to teach or suggest either of the claimed steps of "responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction" and "enabling counting of each event associated with execution of the instruction if the indicator is associated with the instruction".

Pardo is directed to a mechanism for implementing watchpoints and breakpoints in a data processing system. In rejecting the claim, the Examiner refers to "the load instruction in fig. 2" and col. 2, lines 30-40 of Pardo as disclosing "responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction". In particular, the Examiner states that col. 2, lines 30-40 of Pardo discloses that "logic circuitry derives (determines) watchpoint conditions from the instructions (i.e. via an indicator)". Applicants respectfully disagree. Col. 2, lines 30-40 of Pardo reads as follows:

> The processor may also include logic circuitry for deriving a watchpoint condition from the instructions and for generating the watchpoint information in dependence on the watchpoint condition. The watchpoint information may include information regarding the incrementing and decrementing of watchpoint counters (e.g. counters **41** and **42** in FIG. **2**), as well as information regarding whether or not a watchpoint has occurred. Alternate embodiments of the present invention may include other information as part of the watchpoint information.

The above recitation states that a watchpoint condition is derived from instructions, and that watchpoint information is generated that may include information regarding the incrementing and decrementing of counters. The above recitation, however, does not disclose or suggest determining if an indicator is associated with an instruction or determining whether an indicator is associated with an instruction "responsive to receiving an instruction at a processor in the data processing system" as recited in claim 1. There does not appear to be an indicator in Pardo, and there is certainly no disclosure or suggestion of "responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction".

Pardo also does not disclose or suggest "enabling counting of each event associated with execution of the instruction if the indicator is associated with the instruction" recited in claim 1. The Examiner refers to col. 2, lines 41-47 of Pardo as disclosing this feature. Col. 2, lines 41-47 of Pardo is as follows:

> In some embodiments of the present invention, the processor also includes a counter for counting the number of watchpoints, wherein each watchpoint includes a value indicative of one

count. If an executed instruction having an associated watchpoint is canceled before it is completed, preferably the count associated with the watchpoint is removed from the counter.

Although the above recitation indicates that a counter may be provided in Pardo to count the number of watchpoints, there is no disclosure or teaching that such counting is enabled "if the indicator is associated with the instruction" as recited in claim 1. Pardo does not discuss how counting of watchpoints is enabled and does not disclose that counting is enabled if an indicator is associated with an instruction. Pardo, accordingly, also does not disclose or suggest "enabling counting of each event associated with execution of the instruction if the indicator is associated with the instruction", and does not anticipate claim 1 for this reason as well.

Claim 1, accordingly, patentably distinguishes over Pardo in its present form, and withdrawal of the rejection thereunder is respectfully requested.

Claim 3 depends from and further restricts claim 1 and is also not anticipated by Pardo at least by virtue of its dependency.

Independent claims 18 and 23 have been amended in a manner similar to claim 1, and are also not anticipated by Pardo for similar reasons as discussed above with respect to claim 1. Claim 20 depends from and further restricts claim 18, and claim 25 depends from and further restricts claim 23. These claims are also not anticipated by Pardo, at least by virtue of their dependency.

Independent claim 15 is as follows:

15. A method in a data processing system for monitoring access to data, the method comprising:
identifying a memory location associated with an indicator; and
enabling counting of events associated with accesses to the memory location.

In rejecting claim 15, the Examiner refers to claim 18 in Pardo, and states that "Pardo is considered to identify a memory location associated with an indicator (the one with the watchpoint) to enable storing of its indication value" Claim 18 of Pardo is as follows:

18. A method for operating a data processor, the data processor having an execution unit and having a buffer for storing processor state information, the data processor executing a program having a plurality of instructions in sequential order, the plurality of instructions in sequential order having a plurality of prior instructions and having a present instruction, the method comprising the steps of:
receiving the present instruction;
determining if a watchpoint is associated with the present instruction;
storing a first processor state value in the buffer, said first processor state value corresponding to the present instruction; and
if the watchpoint is associated with the present instruction, storing a watchpoint occurrence indication value in the buffer;
determining that the present instruction has completed execution and that the plurality of prior instructions have also completed execution;

issuing the watchpoint after said step of determining that the present instruction has completed execution and that the plurality of prior instructions have also completed execution.

Applicants are unable to identify any disclosure in claim 18 of Pardo or elsewhere that a memory location associated with an indicator is identified or that events associated with accesses to the identified memory location are counted. Pardo does not disclose the subject matter recited in claim 15, and claim 15 patentably distinguishes over Pardo in its present form.

Claim 17 depends from and further restricts claim 15 and is also not anticipated by Pardo, at least by virtue of its dependency. Independent claim 22 recites similar subject matter as claim 15 and is also not anticipated by Pardo for similar reasons as discussed above with respect to claim 15.

Therefore, the rejection of claims 1-3, 15, 17, 18-20 and 22-25 under 35 U.S.C. § 102 has been overcome.

III. 35 U.S.C. § 103, Obviousness

The Examiner has rejected claims 4-14, 16 and 21 under 35 U.S.C. § 103(a) as being unpatentable over Pardo in view of Merten et al., A Hardware-Driven Profiling Scheme for Identifying Program Hot Spots to Support Runtime Optimization, IEEE, 1999, pp. 136-147 (hereinafter "Merten"). This rejection is respectfully traversed.

In rejecting the claims, the Examiner acknowledges that Pardo does not disclose a system utilizing a cache as specified in claims 4-14, 16 and 21 and cites Merten as teaching "the feature to detect cache misses". The Examiner states that it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the cache feature taught by Merten in the system of Pardo.

Claims 4-10 depend from and further restrict claim 1. Merten does not supply the deficiencies in Pardo as described above. Claims 4-10, accordingly, patentably distinguish over Pardo in view of Merten, at least by virtue of their dependency.

In addition, Applicants respectfully submit that the Examiner has not established a *prima facie* case of obviousness in rejecting the claims. A fundamental notion of patent law is the concept that invention lies in the new combination of old elements. Therefore, a rule that every invention could be rejected as obvious by merely locating each element of the invention in the prior art and combining the references to formulate an obviousness rejection is inconsistent with the very nature of "invention." Consequently, a rule exists that a combination of references made to establish a *prima facie* case of obviousness must be supported by some teaching, suggestion, or incentive contained in the prior art which would have led one of ordinary skill in the art to make the claimed invention.

The Examiner bears the burden of establishing a *prima facie* case of obviousness based on the prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780

(Fed. Cir. 1992). The requirements for establishing a *prima facie* case of obviousness in view of a combination of references are set forth in detail in Section 2142 of the MPEP and include the requirements that the Examiner explain in detail why the combination of the teachings is proper, that the Examiner provide a clear and convincing line of reasoning as to why an artisan would have found the claimed invention obvious in light of the teachings of the references, and that the Examiner provide a showing that it is the prior art and not the Applicants' own disclosure that teaches the combination asserted by the Examiner.

In rejecting the claims, the Examiner asserts only that it would have been obvious to combine the teachings of Pardo and Merten to speed memory accesses and reduce the number of cache misses. The Examiner has not indicated, however, where the cited references suggest the asserted combination, nor has the Examiner provided a clear showing that it is the prior art and not the Applicants' own disclosure that teaches the combination asserted by the Examiner. Accordingly, Applicants respectfully submit that the Examiner has not established a *prima facie* case of obviousness in rejecting the claims as being obvious over Pardo in view of Merten.

In addition, various ones of claims 4-10 recite further subject matter that is neither disclosed nor suggested by Pardo or Merten or their combination. With respect to claim 6, for example, Applicants respectfully disagree with the Examiner's assertion that the purpose of the spare bit in the claim is not clear. Claim 6 clearly specifies that the instruction recited in claim 1 is received in a bundle by an instruction cache in the processor, and that the indicator comprises at least one spare bit in a field in the bundle. As disclosed, for example, on page 26, line 20 to page 27, line 14 of the present specification, spare bits within bundle 500 illustrated in Figure 5 are used to hold indicators 510, 512 and 514.

Applicants respectfully submit that the "at least one spare bit" recited in claim 6 is a positively recited limitation that cannot be simply ignored in rejecting the claims. Neither Pardo nor Merten discloses this feature, and claim 6 patentably distinguishes over the cited art in its own right as well as by virtue of its dependency.

Independent claim 11, together with claims 12-14 dependent thereon, also patentably distinguishes over Pardo in view of Merten. As indicated above, Merten does not supply the deficiencies in Pardo described in detail with respect to claim 1, and claims 11-14 patentably distinguish over the cited art in their present form.

Claim 16 depends from and further restricts claim 15, and claim 21 depends from and further restricts claim 18. These claims also patentably distinguish over the cited art, at least by virtue of their dependency.

Therefore, the rejection of claims 4-14, 16 and 21 under 35 U.S.C. § 103(a) as being unpatentable over Pardo in view of Merten has been overcome.

IV. 35 U.S.C. § 103, Obviousness

The Examiner has further rejected claims 4-14, 16 and 21 under 35 U.S.C. § 103(a) as being unpatentable over Pardo in view of Ammons et al., Exploiting Hardware Performance Counters with Flow and Context Sensitive Profiling, ACM, 1997, pp. 85-96 (hereinafter "Ammons"). This rejection is respectfully traversed.

In rejecting the claims, the Examiner again acknowledges that Pardo does not disclose a system utilizing a cache as specified in claims 4-14, 16 and 21 and cites Ammons as teaching "the feature to detect cache misses". The Examiner states that it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the cache feature taught by Ammons.

Ammons also does not supply the deficiencies in Pardo as discussed in detail above with respect to claim 1. For similar reasons as discussed above with respect to the rejection of the claims as being unpatentable over Pardo in view of Merten, claims 4-14, 16 and 21 also patentably distinguish over Pardo in view of Ammons.

Therefore, the rejection of claims 4-14, 16 and 21 under 35 U.S.C. § 103(a) as being unpatentable over Pardo in view of Ammons has been overcome.

V. Conclusion

For at least all the above reasons, claims 1, 3-18, 20-23 and 25 patentably distinguish over the cited art and are allowable in their present form. This application is, accordingly, believed to be in condition for allowance, and it is respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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